CHAPTER-10. ELECTRICAL CIRCUIT THEORY

[1] The period of the signal \( x(t) = 8 \sin (0.8\pi t + \pi /4) \) is [GATE 2010]
   A. 0.4\( \pi \)s
   B. 0.8\( \pi \)s
   C. 1.25s
   D. 2.5s

[2] The switch in the circuit has been closed for a long time. It is opened at \( t=0 \). At \( t=0^+ \), the current through the 1\( \mu \)F capacitor is [GATE 2010]

   ![Circuit Diagram]

   A. 0A
   B. 1A
   C. 1.25A
   D. 5A

[3] The second harmonic component of the periodic waveform given in the figure has an amplitude of [GATE 2010]

   ![Waveform Diagram]

   A. 0
   B. 1
   C. \( 2/\pi \)
   D. \( \sqrt{5} \)

[4] As shown in the figure, a 1 resistance is connected across a source that has a load line \( v+i=100 \). The current through the resistance is [GATE 2010]

   ![Source Diagram]

   A. 25A
   B. 50A
   C. 100A
   D. 200A

[5] If the 12\( \Omega \) resistor draws a current of 1A as shown in the figure, the value of resistance \( R \) is [GATE 2010]

   ![Resistor Diagram]

   A. 4\( \Omega \)
   B. 6\( \Omega \)
   C. 8\( \Omega \)
   D. 18\( \Omega \)
[5] If the electrical circuit of figure (b) is an equivalent of the coupled tank system of figure (a), then [GATE 2010]

A. A,B are resistances and C,D capacitances
B. A,C are resistances and B,D capacitances
C. A,B are capacitances and C,D resistances
D. A,C are capacitances and B,D resistances

[7] The two-port network P shown in the figure has ports 1 and 2, denoted by terminals (a,b) and (c,d), respectively. It has an impedance matrix $Z$ with parameters denoted by $Z_{ij}$. A 1Ω resistor is connected in series with the network at port 1 as shown in the figure. The impedance matrix of the modified two-port network (shown as a dashed box) is [GATE 2010]

$$
\begin{align*}
(Z_{11} + 1) & \begin{pmatrix} 1 & Z_{12} + 1 \\ Z_{21} + 1 & Z_{22} + 1 \end{pmatrix} \\
(Z_{21} + 1) & \begin{pmatrix} Z_{11} + 1 & Z_{12} \\ Z_{21} + 1 & Z_{22} + 1 \end{pmatrix} \\
\end{align*}
$$

A. $\begin{pmatrix} Z_{11} + 1 & Z_{12} \\ Z_{21} + 1 & Z_{22} + 1 \end{pmatrix}$
B. $\begin{pmatrix} Z_{11} + 1 & Z_{12} \\ Z_{21} + 1 & Z_{22} + 1 \end{pmatrix}$
C. $\begin{pmatrix} Z_{11} + 1 & Z_{12} \\ Z_{21} + 1 & Z_{22} + 1 \end{pmatrix}$
D. $\begin{pmatrix} Z_{11} + 1 & Z_{12} \\ Z_{21} + 1 & Z_{22} + 1 \end{pmatrix}$

Ans:C

[8] The Maxwell’s bridge shown in the figure is at balance. The parameters of the inductive coil are [GATE 2010]

$$
\begin{align*}
R & = R_2 R_3 / R_4, L = C_4 R_2 R_3 \\
L & = R_2 R_3 / R_4, R = C_4 R_2 R_3 \\
R & = R_2 R_3 / R_4, L = 1(C_4 R_2 R_3) \\
L & = R_2 R_3 / R_4, R = 1/(C_4 R_2 R_3)
\end{align*}
$$

A. $R = R_2 R_3 / R_4, L = C_4 R_2 R_3$
B. $L = R_2 R_3 / R_4, R = C_4 R_2 R_3$
C. $R = R_2 R_3 / R_4, L = 1(C_4 R_2 R_3)$
D. $L = R_2 R_3 / R_4, R = 1/(C_4 R_2 R_3)$
Statement:

The L-C circuit shown in the figure has an inductance L=1mH and a capacitance C=10μF

The initial current through the inductor is zero, while the initial capacitor voltage is 100 V. The switch is closed at t=0. The current i through the circuit is: [GATE 2010]

- A. 5cos(5x10^3 t)A
- B. 5sin(10^4 t)A
- C. 10cos(5x10^3 t)A
- D. 10sin(10^4 t)A

The L-C circuit of statement is used to commutate a thyristor, which is initially carrying a current of 5A as shown in the figure below. The values and initial conditions of L and C are the same as in statement. The switch is closed at t=0. If the forward drop is negligible, the time taken for the device to turn off is [GATE 2010]

- A. 52μs
- B. 156μs
- C. 312μs
- D. 26μs

The voltage applied to a circuit is 100√2 cos(100πt) volts and the circuit draws a current of 10√2sin(100πt +π/4) amperes. Taking the voltage as the reference phasor, the phasor representation of the current in amperes is [GATE 2011]

- A. 10√2∠-π/4
- B. 10∠-π/4
- C. 10∠+π/4
- D. 10√2∠+π/4

A reactance network in the Foster's I form has poles at ω=∞(infinity). The element in box-1 in the above network is [IES2010]
A. a capacitor
B. an inductor
C. a parallel LC circuit
D. a series LC circuit

Statement for Linked Answer Questions 12 and 13: [GATE 2009]

[12] For the circuit given above, the Thevinin’s resistance across the terminals A and B is [GATE 2009]
   A. 0.5kΩ
   B. 0.11kΩ
   C. 1kΩ
   D. 0.5kΩ

[13] For the circuit given above, the Thevenin’s voltage across the terminals A and B is [GATE 2009]
   A. 1.25V
   B. 0.25V
   C. 1V
   D. 0.5V

[14] For the circuit shown, find out the current flowing through the 2Ω resistance. Also identify the changes to be made to double the current through the 2Ω resistance. [GATE]

A. (5A;Put Vs=20V)
B. (2A;Put Vs=8V)
C. (5A;Put Vs=10A)
D. (7A;Put Vs=12A)

[15] The common emitter forward current gain of the transistor shown is 100. The transistor is operating in [GATE 2007]
A. Saturation Region  
B. Cutoff Region  
C. Reverse active region  
D. Forward active region  

[16] The three–terminal linear voltage regulator is connected to a 10 ohm load resistor as shown in the figure. If Vin is 10V, what is the power dissipated in the transistor [GATE 2007]

\[ P = \frac{V_1^2}{R_L} \]

A. 0.6W  
B. 2.4W  
C. 4.2W  
D. 5.4W  

**Carry Two Marks Each Statement for Linked Answer Questions: 17 & 18**

In the circuit shown, the three voltmeter readings are \( V_1 = 220V, V_2 = 122V, V_3 = 136V \)

\[ P = \frac{V_1^2}{R_b} \]

[17] The power factor of the load is [GATE2012]  
\[ a. 0.45 \]  
\[ b. 0.50 \]  
\[ c. 0.55 \]  
\[ d. 0.60 \]  

[18] If \( R_L = 5\Omega \), the approximate power consumption in the load is [GATE2012]  
\[ a. 700W \]  
\[ b. 750W \]  
\[ c. 800W \]  
\[ d. 850W \]  

**Common Data Questions: 19&20**

With 10V dc connected at port A in the linear nonreciprocal two-port network shown below, following were observed:

1. 1Ω connected at port B draws a current of 3A  
2. 2.5Ω connected at port B draws a current of 2A  

\[ V = I \times R \]
[19] For the same network, with 6V dc connected at port A, 1Ω connected at port B draws $\frac{7}{3}$ A. If 8V dc is connected to port A, the open circuit voltage at port B is [GATE2012]
   a. 6V  
   b. 7V  
   c. 8V  
   d. 9V

[20] With 10V dc connected at port A, the current drawn 7Ω connected at port B is [GATE2012]
   a. $\frac{3}{7}$A  
   b. $\frac{5}{7}$A  
   c. 1A  
   d. $\frac{9}{7}$A

[21] A balanced RYB-sequence, Y-connected (Star Connected) source with $V_{RN}=100$ volts is connected to a Δ-connected (Delta connected) balanced load of (8+j6) ohms per phase. Then the phase current and line current values respectively, are [IES2010]
   A. 10A; 30A  
   B. $10\sqrt{3}$A; 30A  
   C. 10A; 10A  
   D. $10\sqrt{3}$A; $10\sqrt{3}$A

[22] Assuming both the voltage sources are in phase, the value of R for which maximum power is transferred from circuit A to circuit B is [GATE2012]

![Circuit A and Circuit B diagram]

   a. 0.8Ω  
   b. 1.4Ω  
   c. 2Ω  
   d. 2.8Ω

[23] The voltage gain $A_v$ of the circuit shown below is [GATE2012]

![Circuit diagram]

   a. $|A_v|\approx200$  
   b. $|A_v|\approx100$  
   c. $|A_v|\approx20$  
   d. $|A_v|\approx10$
[24] If $V_A - V_B = 6V$, then $V_C - V_D$ is \[ \text{[GATE2012]} \]

-5V, 2V, 3V, 6V

**Solution Hint:**
As $V_A - V_B = 6 \Rightarrow I = V/R = 6/2 = 3A$
entering current = leaving current [KCL]
so current from $V_D$ to $V_C$ is same as 3A
convert the current source to voltage source
$V = IR = 2 \times 1 = 2V$

$$V = V_C + 2V + (3 \times 1)V = V_C + 5V$$

$V_C - V_D = -5V$

[25] The circuit shown is a \[ \text{[GATE2012]} \]

a. Low pass filter with $f_{3dB} = \frac{1}{(R_1 + R_2)C} \text{ rad/s}$
b. High pass filter with $f_{3dB} = \frac{1}{(R_1C)} \text{ rad/s}$
c. Low pass filter with $f_{3dB} = \frac{1}{(R_1C)} \text{ rad/s}$
d. High pass filter with $f_{3dB} = \frac{1}{(R_1 + R_2)C} \text{ rad/s}$

[6] In the circuit shown, an ideal switch S operated at 100kHz with a duty ratio of 50%. Given that $\Delta i_c = 1.6A$ peak-to-peak and $I_0$ is 5A dc, the peak current in $S$ is \[ \text{[GATE2012]} \]
a. 6.6A  
b. 5.0A  
c. **5.8A**  
d. 4.2A  

**Solution Hint:**  
\[ \Delta i_c = 1.6\text{A peak-to-peak} \]  
The positive peak = \( \Delta i_c / 2 \)  
The current flows through the switch has a peak of = \( io + \Delta i_c / 2 \)  
For your information... The current waveform is like this

The lowest point will be 5A... highest point will be 5+ 0.8

[27] The i-v characteristics of the diode in the circuit given below are  
i = \{ \begin{array}{ll}  
V - 0.7 /500\text{A}, & V \geq 0.7 \text{V} 
0\text{A}, & V < 0.7 \text{V} 
\end{array} \}

The current in the circuit is [GATE 2012]

\[ \text{a. 10 mA} \]  
\[ \text{b. 9.3 mA} \]  
\[ \text{c. 6.67 mA} \]  
\[ \text{d. 6.2 mA} \]

**Sol. Hint:**  
we have to find \( v \) and then apply in ct. equ...  
KVL...10 = 1K * \( i + v \)  
10 = 1000i +v = 1000(v-0.7/500) + v  
solve it... \( v = 0.8 \ldots \)

[8] In the following figure, \( C_1 \) and \( C_2 \) are ideal capacitors. \( C_1 \) has been charged to 12V before the ideal switch \( S \) is closed at \( t=0 \). The current \( i(t) \) for all \( t \) is [GATE 2012]
a. Zero  

b. A step function  
c. An exponentially decaying function  
d. An impulse function  

**Sol. Hint:**  
If it is RC ckt...ie any Resistance in series with capacitor, it will be an exponentially decaying function...here no resistance...so charge instantly...ie impulse function...  

[9] The impedance looking into nodes 1 and 2 in the given circuit is [GATE 2012]  

![Circuit Diagram](image1)

a. 50 Ω  
b. 100 Ω  
c. 5 KΩ  
d. 10.1 KΩ  

**Ans:** A  
**Answer**

[10] In the circuit given below, the current through the inductor is [GATE 2012]  

![Circuit Diagram](image2)

a. \((2/1+j)A\)  
b. \((-1/1+j)A\)  
c. \((1/1+j)A\)  
d. 0A  

**Sol Hint:** consider top half of the circuit  
R & L are in parallel with ct. source...other end connected to low potential...ie GND... convert ct. to V source...: